Exhibit L

1 **PRUETZ LAW GROUP LLP**
Adrian M. Pruetz (Bar No. 118215)
2 ampruetz@pruetzlaw.com
Erica J. Pruetz (Bar No. 227712)
3 ejpruetz@pruetzlaw.com
200 N. Sepulveda Blvd., Suite 1525
4 El Segundo, CA 90245
Phone: 310.765.7650
5 Fax: 310.765.7641

6

7 **LEE TRAN & LIANG APLC**
Enoch H. Liang (Bar No. 212324)
8 ehl@ltlcounsel.com
Steven R. Hansen (Bar No. 198401)
9 srh@ltlcounsel.com
601 S. Figueroa Street, Suite 4025
10 Los Angeles, CA 90017
Phone: 213.612.3737
11 Fax: 213.612.3773

12

Attorneys for Defendant and
13 Counterclaimant
NETLIST, INC.
14

UNITED STATES DISTRICT COURT
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NORTHERN DISTRICT OF CALIFORNIA
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OAKLAND DIVISION
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18 | GOOGLE INC., | CASE NO. C-08-04144 SBA |
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| Plaintiff, | **DEFENDANT NETLIST, INC.'S** |
20 | | **OPENING CLAIM CONSTRUCTION** |
| v. | **BRIEF** |
21 | | |
| NETLIST, INC., | Date: November 12, 2009 |
22 | | Time: 9:00 a.m. |
| Defendant. | Place: Courtroom 3, 3rd Floor |
23 | | Judge: Hon. Saundra Brown Armstrong |
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INTRODUCTION

This case concerns Google"s infringement of Netlist"s U.S. Patent No. 7,289,386 (the ""386 Patent"), which is directed to a novel computer memory module that avoids the memory limitations of many commercial computers and servers, while also providing a significant reduction in the energy consumed to store information in memory. The asserted claims include a printed circuit board and a logic element. The logic element receives control and computer signals from the host computer in which the memory module is installed and translates signals provided for a limited number of memory devices into signals for an expanded number of memory devices. Embodiments of the claimed invention allow for the use of lower density memory chips, which are more cost effective and provide a lower cost per bit of memory storage.

The parties" core claim construction disputes concern the terms "logic element," "control signals," and "command signals." In accordance with the Federal Circuit"s well-established canons of claim construction, Netlist"s proffered constructions are based on the intrinsic evidence (claim language, specification, and file history) and provide the ordinary meaning of these terms as understood by those skilled in the art. Thus, Netlist defines "logic element" as "a hardware circuit that performs a predefined function on input signals and presents the resulting signals as its output." Netlist defines "control signals" as "signals, including address and command signals, that regulate system operations." Netlist defines "command signals" as "signals, such as a read, write, refresh, or precharge signal, that initiates a predetermined type of computer operation."

In sharp contrast, Google"s proffered constructions run afoul of the canons of claim construction and seek to limit Netlist"s claims in a manner that finds no support in the intrinsic record or in Federal Circuit precedent. Google first attempts to obscure the individual meanings of "logic element," "control signals," and "command signals" by requesting a construction of the

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phrase "logic element receiving a set of input control signals from the computer system." Google uses this linguistic sleight of hand to import a requirement that the computer system provide signals "directly" to the logic element, notwithstanding the absence of any intrinsic support for such a limitation.

Google next seeks to limit the definitions of "control signals" and "command signals" by limiting the terms to a particular mechanical structure used to transmit the signals: pins. Again, there is no support in the intrinsic evidence for this limitation. Perhaps, Google will try to introduce extrinsic evidence in the form of expert testimony to support its constructions, but the Federal Circuit prohibits resort to extrinsic evidence when a claim term can be construed based on the intrinsic record alone. As Netlist"s constructions are fully supported by the intrinsic record, the Court should adopt Netlist"s constructions in their entirety.

THE '386 PATENT

The „386 Patent issued on October 30, 2007 from an application claiming priority back to 2004.[1] Pruetz Decl., Exh. A: the „386 Patent. The patent is directed to memory modules capable of expanding the number of memory devices that can be utilized by a computer. The individual memory chips on which information is stored can be combined into discrete sets or "ranks" to effectively increase the capacity of the memory module. The „386 Patent explains how these ranks are used to increase capacity as follows:

> The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. For example, a memory module with four ranks has double the memory capacity of a memory module with two ranks and four times the memory capacity of a memory module with one rank.

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[1] For the Court"s convenience, the „386 Patent is attached as Exhibit A to the Declaration of Adrian M. Pruetz ("Pruetz Decl.").

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Pruetz Decl., Exh. A; the ,386 Patent at 2:23-30. Put differently, a given total amount of memory may be provided by using a small number of high density memory devices or a large number of low density memory devices. As the patent explains, it is economically advantageous to use the latter approach because the memory devices are significantly less expensive:

> Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM devices) are *much more than twice* the price of lower-density DRAM devices (e.g., 512 Mb DRAM devices). In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower density DRAM devices.

Id. at 4:64-5:2.

Unfortunately, many computers are unable to exploit the economic benefits of lower density memory devices because they are limited in the number of ranks that they can utilize:

> Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each slot is limited.
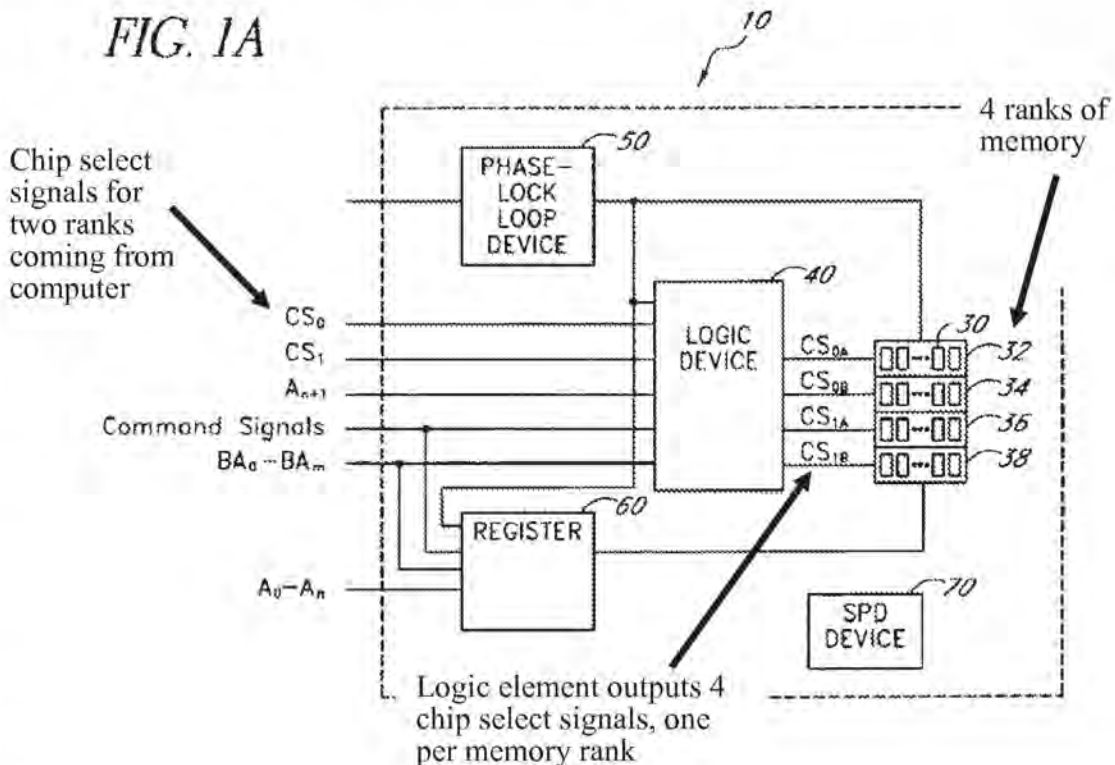
Id. at 2:38-42. This limitation is particularly significant for large, memory-intensive server computers, such as data center servers and cloud computing servers. In the case of such larger computers, it is often desirable to maximize overall memory capacity to improve performance by using as many high density memory chips as can be utilized by the computer.

It is against this backdrop that the claimed invention of the ,386 Patent was developed. Claim 1 of the patent describes a memory module comprising a printed circuit board, a logic element, and a plurality of memory devices arranged in ranks. As the text of the claim indicates, the logic element receives control and command signals from the computer system which correspond to the limited number of ranks to which the computer outputs signals and then outputs signals corresponding to the actual number of ranks on the module:

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1.   A memory module connectable to a computer system, the memory module comprising: a printed circuit board; a plurality of memory devices coupled to the printed circuit board, the plurality of memory devices having a first number of memory devices; and a logic element coupled to the printed circuit board, the logic element receiving a set of input control signals from the computer system, the set of input control signals corresponding to a second number of memory devices smaller than the first number of memory devices, the logic element generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of memory devices, wherein the plurality of memory devices are arranged in a first number of ranks, and the set of input control signals corresponds to a second number of ranks of memory modules, the second number of ranks less than the first number of ranks, wherein the logic element further responds to a first command signal from the computer system by generating a second command signal transmitted to the plurality of memory devices, the first command signal corresponding to the second number of ranks and the second command signal corresponding to the first number of ranks.

Figure 1A illustrates an embodiment of the claimed invention and shows how control signals known as "chip-select signals," which correspond to two ranks (CSo and CS1 for rank 0 and rank 1), are translated into control signals corresponding to four ranks (CS_{oA}, CS_{oB}, CS_{1A}, CS_{1B} for ranks 0A, 0B, 1A, and 1B, respectively):

FIG. 1A

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1 Each of the embodiments of the logic device 40 receives a set of input signals in response

2 to which output signals are generated. For example, the „386 Patent states that: "The logic

3 element 40 generates a set of output control signals in response to a set of input control signals."

4 Pruetz Decl., Exh. A; the „386 Patent at 5:23-25. The patent goes on to explain to one of ordinary

5 skill in the art how to construct a logic element using a number of different hardware circuits or

6 electrical component configurations as a logic device:

7

8   In certain embodiments, the logic element 40 comprises a programmable-logic
     device (PLD), an application specific integrated circuit (ASIC), a field
9   programmable gate array (FPGA), a custom-designed semi-conductor device, or a
     complex programmable logic device (CPLD).
        * * *
10   In certain embodiments, the logic element 40 comprises various discrete electrical
     elements, while in certain other embodiments, the logic element 40 comprises one
11   or more integrated circuits. Persons skilled in the art can select an appropriate logic
     element 40 in accordance with certain embodiments described herein.
12

13 Pruetz Decl., Exh. A; the „386 Patent at 6:47-62.

14 The patent describes embodiments of "control signals" and "command signals" as follows:

15
     As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic
16   element 40 receives a set of input control signals, which includes address signals
     (e.g., bank address signals, row address signals, column address signals, gated
17   column address strobe signals, chip-select signals) and command signals (e.g.,
     refresh, precharge) from the computer system. In response to the set of input
18   control signals, the logic element 40 generates a set of output control signals which
     includes address signals and command signals.
19
   Id. at 6:63-7:5.
20

21   In certain embodiments of the invention, the logic element includes computer code to

22 translate signals provided on the basis of the smaller number of ranks utilized by the computer

23 system to the larger number of ranks actually employed in the memory module. *Id.* at 14:21-

24 17:33.

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ARGUMENT

I. LEGAL STANDARD

The Federal Circuit's *en banc* decision in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005), lays out the framework for claim construction analysis. Generally, a claim term has its ordinary and customary meaning—the meaning of the term to a person of ordinary skill in the art. *Id.* at 1312-13; *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). The Federal Circuit classifies claim construction evidence into two categories, intrinsic and extrinsic. Intrinsic evidence consists of the claim language, specification, and file history. *Vitronics*, 90 F.3d at 1582.   Extrinsic evidence consists of evidence outside the patent document and file history, including dictionaries, learned treatises and expert testimony. *Id.* at 1584. However, the Federal Circuit has "viewed extrinsic evidence in general as less reliable than the patent and its prosecution history in determining how to read claim terms." *Phillips*, 415 F.3d at 1318. Moreover, it is improper to base a claim construction on extrinsic evidence if the intrinsic evidence is sufficient to construe the claim. *Vitronics*, 90 F.3d at 1584 ("Only if there were still some genuine ambiguity in the claims, after consideration of all available intrinsic evidence, should the trial court have resorted to extrinsic evidence, such as expert testimony, in order to construe claim 1").

The specification "is always highly relevant to the claim construction analysis," *Phillips*, 415 F.3d at 1315 (citations omitted). However, it is improper to limit the claims to unclaimed aspects of the specification embodiments, a practice known as "importing" limitations. *Liebel-Flarshiem v. Medrad*, 348 F.3d 898, 906 (Fed. Cir. 2004)

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II. THE COURT SHOULD ADOPT NETLIST'S CONSTRUCTIONS IN THEIR ENTIRETY

For the reasons set forth below, the Court should adopt Netlist"s proffered constructions in their entirety. Google"s constructions seek to limit the asserted claims not only to aspects of the preferred embodiments, but in some cases, to features that appear *nowhere* in the „386 Patent.

A. Logic Element

The parties" central dispute over the construction of this term concerns Google"s improper attempt to limit "logic element" to require the receipt of signals "directly" from the computer system. Joint Claim Construction and Prehearing Statement at 1 (Document 33-2). Netlist submits that the proper construction for "logic element" is "**a hardware circuit that performs a predefined function on input signals and presents the resulting signals as its output.**" Google apparently does not dispute the "hardware circuit" portion of Netlist"s construction, as it includes the phrase "electronic circuitry" in its own construction.

The claim language supports Netlist"s construction. Claim 1 describes the logic element as "receiving a set of input control signals from the computer system" and "generating a set of output control signals in response to the set of input control signals." Pruetz Decl., Exh. A; the „386 Patent at 33:31-48. The claim also makes clear that the logic element performs a predefined function on the input signals because it provides output signals that correspond to a different number of memory ranks than the input signals correspond to. *Id.* at 33:31-44.

Each embodiment of the „386 Patent describes the "logic element" as generating a set of output signals from a set of input signals. For example, the specification states that the "logic element 40 generates a set of output control signals in response to the set of input control signals." Pruetz Decl., Exh. A; the „386 Patent at 5:23-25. Other portions of the specification are in accord. *See e.g., id. at* 7:2-5, 11:53-38, and 11:63-12:1. Additional specification excerpts provide

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examples of the pre-defined function that the logic element performs on the signals it receives, e.g., "The logic element 40 translates the first set of address signals and control signals into a second set of address and control signals. . . ." *Id.* at 22:44-47. Technical dictionaries, a preferred category of extrinsic evidence, are in accord with Netlist"s construction. For example, the *Mc-Graw Hill Dictionary of Scientific and Technical Terms* defines logic element as: "A hardware circuit that performs a simple, predefined transformation on its input and presents the resulting signal as its output. Occasionally known as functor." *Mc-Graw Hill Dictionary of Scientific and Technical Terms* (6th ed. 2003) at 1232; Pruetz Decl., Exh. B.

Nowhere does the patent specification describe the logic element as "directly" receiving signals from the computer system. Recognizing this fact, Google seeks to obscure the proper construction of "logic element" by seeking a construction of the phrase "logic element receiving a set of input control signals from the computer system" in order to suggest a structural relationship between the signals and the logic element. However, nothing in the patent suggests that the phrase Google seeks to arbitrarily extract from a larger context and construe has any specialized meaning that would justify its construction apart from the individual terms that comprise it. Moreover, nowhere does the patent indicate that a logic element is defined by the manner in which it is physically connected to the computer that provides signals to it. Even the JEDEC standard cited by Google lacks the "directly" feature Google seeks to import into claim 1. Joint Claim Construction and Prehearing Statement at 8 (Document 33-2).

In view of the foregoing, Google may seek to offer expert testimony to support its construction of "logic element receiving a set of input control signals from the computer system. " However, because the specification and claim language is sufficient to resolve the construction of "logic element," such evidence would be improper and should be excluded. *Vitronics*, 90 F.3d at

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1584. Google"s citations to the specification and extrinsic evidence do not support its proffered construction, but in any event, they constitute an improper attempt to import unclaimed features into the claims.

B. Rank

Netlist submits that the proper construction for "rank" is "**a row of memory devices**." The specification establishes and consistently uses this definition for "rank." For example, the specification states that "DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width." Pruetz Decl., Exh. A; the ,386 Patent at 2:16-19. The specification does not use "rank" to refer to anything other than memory devices, yet Google"s definition ignores this fact.

C. Signal

The parties" dispute concerning this term centers on Google"s improper attempt to define "signal" as a particular mechanical structure used to transmit or receive a signal: "pins." "Signal" is a straightforward term that does not require construction. However, if the Court is inclined to construe the term, Netlist submits that the construction should be "**an event or phenomenon that conveys information from one point to another**." This construction, taken from the *Institute of Electrical and Electronics Engineers (IEEE) Standard Dictionary of Electrical and Electronics Terms* (6th ed.), comports with the ordinary and customary understanding of the term "signal". Pruetz Decl., Exh. C.

The specification does not expressly define "signal." However, its use of the term indicates that a signal is an event or phenomenon that conveys information from one point to another. As discussed below, the term "control signals" is used in the specification to describe an event or phenomenon that conveys bank address information, row address information, column address information, etc. Pruetz Decl., Exh. A; the ,386 Patent at 6:64-7:5. Similarly, the

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specification uses "command signal" to convey information about certain computer operations such as read, write, refresh, or precharge. The specification is replete with references to "signals" that make no mention of the use of pins. *See, e.g., id.* at 2:34-38, 5:36-41, 6:64-7:5.

Google seeks to improperly limit the scope of "signal" to "information presented on one or more *pins of a device dedicated for that specific* information" (emphasis added). First, whether signals are transmitted via pins or any other specific connection has no bearing on the meaning of "signal" itself.

Second, by requiring pins that are "dedicated. . . for specific information," Google"s definition of "signals" effectively seeks to limit the ,386 Patent claims to those logic elements that have pre-defined and assigned pins for specific types of signals. However, Google does not and cannot cite to any portion of the specification that indicates such a hardware configuration is required.

Third, Google selectively relies on only one portion of the ,386 Patent specification that even mentions pins. That portion of the specification is limited to embodiments that include data strobe signal pins or "DQS" pins and data output pins or "DQ" pins. Pruetz Decl., Exh. A; the ,386 Patent at 29:58-63 and 31:65-32:11. Those few exemplary embodiments have no bearing on the meaning of "signal" much less support Google"s construction.

D. Command Signal, Chip-Select Signal; Control Signal

Google"s proposed constructions of each of these terms are infected with its flawed construction of "signal," as discussed above. For this reason alone, they should be rejected. In addition, Google"s constructions circularly define the "command," "chip-select," and "control" portions, respectively, of these terms and therefore will not aid the jury.

1. Command Signal

The proper construction of "command signal" is "**a signal, such as a read, write, refresh,**

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or precharge signal, that initiates a predetermined type of computer operation."

This construction flows directly from the specification. The specification states that command signals "define operations such as refresh, precharge, and other operations." Pruetz Decl., Exh. A; the ,386 Patent, Table 1, n.4. The specification also includes "activation, read, [and] write" as examples of command signals. *Id.* at 8:48. Each of these examples supports Netlist"s construction.

Netlist"s construction is also consistent with the technical dictionary definitions of "command signal". *See IEEE* at 178 ("A pulse, signal, or set of signals initiating one step in the performance of a controlled operation.); *McGraw Hill* at 438 ("A signal that initiates a predetermined type of computer operation that is defined by an instruction") Pruetz Decl., Exhs. B and C.; *Phillips*, 415 F.3d at 1318 (noting that technical dictionaries are especially useful in determining the meaning of terms to those of skill in the art).

In contrast, Google seeks to define "command signals" as "signals presented on control pins of the logic element." The structure on which command signals are presented (e.g., pins) has no bearing on the meaning of "command signals." At best, Google"s construction is an improper attempt to limit the claims to a few isolated examples concerning DQS and DQ pins from the ,386 Patent"s specification, ignoring many others. Moreover, Google"s construction circularly references the word "command," and therefore, will be unhelpful to the Court and the jury.

2. Chip-Select Signal

This term is recited in claim 11, which depends from claim 1. The proper construction of "chip-select signal" is "**an address signal that enables the input and output of data to and/or from memory devices.**"

The specification supports this construction. It explains that "[d]uring operation, the ranks of memory modules are selected or activated by control signals that are received from the

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processor. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals." The specification also describes "chip-select signal" as a type of address signal. Pruetz Decl., Exh. A; the „386 Patent at 5:36-40; 6:63-7:1. Thus, the specification establishes that "chip-select signal" refers to an address signal that "activates" memory devices, thereby enabling the input and output of data to and/or from them.

Proceeding from its flawed construction of "signal," Google defines "chip-select signal" as "signal presented on chip-select pins of the logic element." Neither of the two specification references cited by Google refer to "chip-select pins." *See* Joint Claim Construction and Prehearing Statement at 34 (Document 33-2).

Google cites JEDEC standard No. 1000B.01 in support of its construction. However, this standard makes no mention of chip-select pins, and in fact, tracks Netlist"s construction:

> chip-select input: A control input that when active, permits operation of the integrated circuit and, when inactive, prevents input or output of data to or from the integrated circuit.

Joint Claim Construction and Prehearing Statement at 35 (Document 33-2). While Google also cites a document called "JESD79F" which mentions chip-select pins, the document does not inform the meaning of "chip-select signal." Moreover, it is impermissible for the Court to consider such extrinsic evidence in view of the fact that "chip-select signal" can be construed from the intrinsic record alone. *Vitronics*, 90 F.3d at 1584.

3. Control Signals

The proper construction for "control signals" is "**signals, including address and command signals, that regulate system operations.**"

This construction flows directly from the specification. For example, the specification states, "the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals . . . chip-select signals) and command signals . . . from the computer

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system." Pruetz Decl., Exh. A; the „386 Patent at 6:64-7:2. This supports Netlist"s construction, which explains that "control signals" refers to particular types of signals, including address and command signals. *See Phillips*, 415 F.3d at 1315-16.

The specification also states that "the ranks of a memory module are selected or activated by control signals that are received from the processor." Pruetz Decl., Exh. A; the „386 Patent at 2:34-36. Each description of "control signals" in the „386 Patent refers to signals that regulate system operations.

Once again, Google defines "control signals" as "signals presented on control pins of the logic element." Joint Claim Construction and Prehearing Statement at 14 (Document 33-2). In the Joint Claim Construction submission, both parties cite the same portions of the specification in support of their proffered constructions. None of them refer to "control pins" on a logic element. Moreover, as with "chip-select signal" and "command signal," Google circularly uses the term "control" in its construction, which does nothing to enlighten the jury.

E. The Set of Input Control Signals Corresponding to a Second Number of Memory Devices Smaller Than the First Number of Memory Devices

Netlist submits that this phrase requires no separate construction apart from its constituent terms such as "control signals" and "memory devices" that are construed elsewhere. As with its effort to limit "logic element," Google seeks a construction of the entire phrase to graft an additional limitation onto the claim, namely, that the computer system be unaware of the actual number of memory devices ("first number of memory devices") present on the memory module. Thus, Google"s definition of this phrase includes the limitation "based on the computer system understanding the memory module to have the second number of devices."

First, Google"s attempt to seek any construction of this phrase is improper since it can be readily be understood based on the constructions of its constituent terms. *See United States*

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1   *Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997) (claim construction is

2   required only when the meaning or scope of technical terms and words of art is unclear and

3   requires resolution).

4   Second, the language of the claim indicates that the "understanding" of the computer

5   system as to the number of memory devices is irrelevant. The claim indicates that the computer

6   provides a set of input signals that "correspond[ ] to a second number of memory devices." Pruetz

7   Decl., Exh. A; the ,386 Patent at 33:33-34. No issue of the "understanding" of the computer

8   system is implicated by this language.

9   Third, at most, the specification excerpts on which Google relies indicate that in certain

10   *embodiments*, the computer is configured for fewer devices than are actually present, and in that

11   sense, understands there to be the lesser (second) number of devices:

12

13   **In certain embodiments**, the memory module 10 simulates a virtual memory
                module when the number of memory devices 30 of the memory module 10 is larger

14   than the number of memory devices 30 per memory module for which the
                computer system is configured to utilize.

15

16   Pruetz Decl., Exh. A; the ,386 Patent at 7:18:29 (emphasis added).

17   If anything, the specification indicates that the inventors contemplated embodiments in

18   which the computer would be aware of the actual number ("first number") of memory devices on

19   the memory module. The specification explains that in many memory modules, a serial-presence-

20   detect (SPD) device communicates "the number of memory devices and the memory density per

21   memory device" to the computer system. *Id.* at 9:31-37. The specification further explains that it

22   is only in "certain embodiments" that this standard configuration is altered so that the SPD

23   "characterize[s] the memory module 10 as having fewer memory devices than the memory module

24   10 actually has . . . . " *Id.* at 10:45-47. This characterization of standard SPDs and their

25

26   modification in only "certain embodiments" clearly indicates that there was no intent on the part

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28   - 14 -

1 of the patent drafter to limit the claims to systems in which the computer "understands" there to be

2 fewer memory devices ("second number") than there actually are ("first number"). "Even when

3 the specification describes only a single embodiment, the claims of the patent will not be read

4 restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using

5 „words or expressions of manifest exclusion or restriction." *Liebel-Flarshiem*, 348 F.3d, at 906.

6 Here, the patent contemplates configurations *other than* those in which the computer understands

7 there to be fewer than the actual number of memory devices. Google"s construction flies in the

8

9 face of and cannot be reconciled with this clear indication of the breadth of the asserted claims.

10   If, notwithstanding the foregoing, the Court is inclined to construe the foregoing phrase,

11 Netlist submits that the proper construction should be "**the set of input control signals received**

12 **from the computer system, which is configured to utilize a memory module having a second**

13 **number of memory devices smaller than the first number of memory devices.**"[2]

14

15   Netlist"s construction of this term is straightforward and supported by the intrinsic

16 evidence. The language of claim 1 indicates that the computer system provides a set of input

17 signals "corresponding" to a number of memory devices (second number) less than the number of

18 memory devices coupled to the printed circuit board (first number). Thus, the claim specifies the

19 manner in which the computer system is configured to utilize a memory module having a second

20 number of memory devices smaller than the first number of memory devices. However, because

21 the relevant constituent terms are already being construed, there is no need to separately construe

22 this phrase.

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25 ——————————————

26 [2] In Exhibit B to the Joint Claim Construction and Prehearing Statement, both parties omitted
the "smaller than the first number of memory devices" limitation from their construction of this

27   (footnote continued)

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F. The First Command Signal Corresponding to the Second Number of Ranks

As with the previous phrase, this phrase needs no separate construction apart from its constituent terms ("command signal" and "ranks") that are construed elsewhere. Again, Google seeks a construction of this phrase to graft an additional limitation requiring the computer system to "understand[ ] the memory module to have the second number of ranks." Joint Claim Construction and Prehearing Statement at 27 (Document 33-2).

The language of the claim concerning the number of ranks makes the "understanding" of the computer system irrelevant. Claim 1 simply requires that the computer system provide input control signals to the logic element that "correspond[ ] to a second number of memory ranks, the second number of memory ranks less than the first number of ranks," wherein the first number of ranks refers to the actual arrangement of the memory devices coupled to the printed circuit board. Pruetz Decl., Exh. A; the ,386 Patent at 33:28-44. No issue of the computer system"s "understanding" concerning the number of ranks is implicated by this language.

Second, in support of its construction, Google points only to specification excerpts that clearly identify *embodiments* of the invention in which the computer system is configured to handle a number of ranks less than the number actually present on the memory module. *See e.g.,* Pruetz Decl, Exh. A; the ,386 Patent at 7:30-67, 8:45-64. However, the specification also indicates that in many memory modules, SPDs communicate to the computer the actual number of ranks present on a memory module, *Id.* at 9:24-37, and that it is only in certain embodiments that this mode of operation is altered so the computer is provided a "virtual" number of ranks which is less than the number actually present. *Id.* at 10:31-35. The only reasonable inference to be drawn

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term. Because construing a claim to omit an express limitation would be improper, Netlist understands this omission to be a mutual oversight and corrects it here.

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1   from these respective portions of the specification is that there was *no intent* to limit the claims in

2   the manner suggested by Google.

3   In the event that the Court construes this term, the proper construction should be "**the first**

4   **command signal received from the computer system, which is configured to utilize a memory**

5   **module having the second number of ranks**."

6   This claim term presents identical issues as the preceding term, and the parties"

7

8   constructions of this term exactly mirror their constructions of the preceding term. Therefore, in

9   the event that this term is construed, for the same reasoning as set forth above, the Court should

10 adopt Netlist"s construction.

11   **G. Number of Ranks of Memory Modules**

12   The proper construction of "number of ranks of memory modules" is "**the common**

13 **number of ranks in which memory devices are arranged on particular memory modules**."

14

15   The specification of the ,386 Patent, and in particular, the figures, makes clear that a given

16 module has a defined number of ranks (e.g, 2 rank, 4 rank). In other words, the number of "ranks"

17 is a property of the memory module. Google"s construction of "ranks" as simply meaning "rows"

18 would mean that this phrase is defined as "number of rows of memory *modules*," a meaning that

19 finds no support in the patent.

20   Context from both the specification and claim makes clear that "number of ranks" refers to

21 a particular characteristic "of memory modules", not to a number of "rows of memory modules."

22

23 For example, the specification repeatedly explains that the way in which memory devices are

24 arranged in ranks is a characteristic of memory modules. Pruetz Decl., Exh. A; the ,386 Patent at

25 2:62-63 ("The memory module comprises a plurality of memory devices arranged in a first

26 number of ranks."); *Id.* at 6:38-43 ("the plurality of memory devices 30 are arranged in a number

27 of ranks.")

28   - 17 -

The specification also makes clear that this characteristic is important, because computer systems are configured to utilize modules that have a certain number of ranks. *Id.* at 7:30-33. Because the patent makes clear that a "rank" is a characteristic property of a memory module, the Court should adopt Netlist"s construction.

<div align="center">

CONCLUSION

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For the reasons provided above, Netlist respectfully requests that the Court adopt Netlist"s claim constructions in their entirety.

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By   /s/ Adrian M. Pruetz
_____
Adrian M. Pruetz
Attorneys for Defendant
Netlist, Inc.

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